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(54) Semiconductor device comprising at least one power transistor and at least one control circuit with dynamic insulation circuit integrated monolithically in the same chip.

(57) In the device there are present a first, second and third switch designed to connect a node of the insulation region with a ground node, the collector or drain of the power transistor and a region of a control circuit transistor respectively. The dynamic insulation circuit of the control circuit comprises a pilot circuit which controls:

- closing of the first switch when the potential of the ground node (or insulation region) is less than the potential of the collector or drain region of the power transistor and the potential of the control circuit region,
- closing of the second switch and opening of the first when the potential of the collector or drain region of the power transistor is less than the potential of the ground node (or the insulation region),
- closing of the third switch and opening of the first when the potential of said control circuit region is less than the potential of the ground node (or the insulation region).

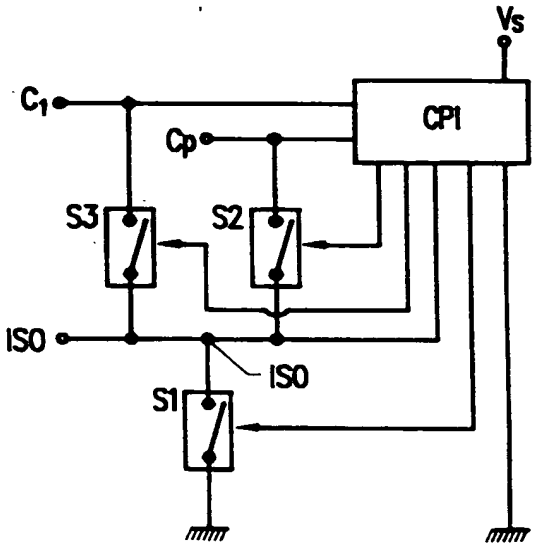

Fig. 4b

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The present invention relates to a semiconductor electronic device with dynamic insulation circuit comprising at least one power transistor and at least one control circuit integrated monolithically in the same chip.

In the chip in which are provided semiconductor electronic devices of the above type there is normally provided an insulation region designed to ensure electric insulation of the individual components and therefore correct operation of the device.

So that said insulation region fulfils this function it is necessary that both junctions of the parasite vertical transistor which said region originates be normally reverse polarized. This is achieved by connecting the insulation region to a potential not greater than the minimum voltage applied to the device.

Therefore, since the terminal with potential lower than the supply battery is normally grounded, the insulation region is also grounded for the above reasons.

However, this provision is not effective in most cases. Indeed, it can happen for example that with switching on the load or spurious pulses on the supplies the voltage (Vout) of the collector (Cp) of the power transistor displays transiently negative values and thus gives rise to so-called 'subground' situations.

To avoid in these cases the parasite vertical transistor going into conduction there has been conceived a dynamic insulation circuit (see French patent application no. 89/16144) which calls for keeping the connection of the insulation region grounded when the Vout is positive and switching the grounding into a connection to the power transistor collector when the Vout displays subground transients.

However, said known dynamic insulation circuit does not allow for the fact that malfunctioning of the insulation region due to going into conduction of said parasite vertical transistor can occur even when negative voltage transients are applied to the control circuit.

The present invention allows achievement of at least the following advantages:

- provision of a semiconductor electronic device with dynamic insulation circuit ensuring insulation conditions even with negative voltage transients on the control circuit,
- reduction of implementation costs of the described dynamic insulation principle by means of integrated structures not requiring a polycrystalline silicon process,
- extension and optimization of the decisional circuitry part dedicated to piloting the synchronous switches which provide the dynamic insulation, and
- dynamic insulation of different insulation regions not connected together with variation of the voltage applied to the common substrate.

The semiconductor electronic device with dynamic insulation circuit in accordance with the present invention comprising at least one power transistor and at least one control circuit integrated monolithically in the same chip has:

- one insulation region designed to insulate the individual components of said control circuit from each other and from the power transistor,
- a first switch designed to connect the insulation region with a ground node,
- a second switch designed to connect the insulation region with the collector or drain of the power transistor,
- a pilot circuit connected with the collector or drain of the power transistor, with the ground node and with said first and second switches which, depending on whether said collector or drain has potential greater or less respectively than that of ground, commands closing of the first or second switch respectively,

and is characterized in that:

- there is present a third switch (S3) designed to connect the insulation region with a region of a control circuit transistor,
- the pilot circuit is connected with said third switch (S3) and with said region of said control circuit transistor and commands closing of the third switch and opening of the first when said region of said control circuit transistor has potential less than that of ground.

Other inventive solutions are indicated below in the claims.

The characteritics of the present invention will be more clear by the following description and the annexed drawings of nonlimiting embodiment examples wherein:

FIG.1 shows an example of a structure comprising a power transistor, a control transistor and an insulation region,

FIG.2 shows an equivalent circuit of the structure of FIG. 1,

FIG.3 shows the basic diagram of a known dynamic insulation circuit,

FIG.4a shows the basic diagram of the dynamic insulation circuit in accordance with the present invention,

FIG.4b shows the basic diagram of the dynamic insulation circuit in accordance with the present invention,

FIG.5 shows the diagram of a realiza-

tion circuit of the circuit CPI of FIG. 4,

FIG.6 shows the basic diagram of the dynamic insulation in accordance with the present invention applied to a solid state 2-way switch,

FIG.7 shows a first example of a realization structure of the switches S1 and S2 of FIGS. 4a and 4b,

FIGS.8 to 11 shows phases of a realization process of the structure of FIG. 7,

FIG.12 shows a second example of a realization structure of the switches S1 and S2 of FIGS. 4a and 4b,

FIG.13 shows a third example of a realization structure of the switches S1 and S2 of FIG. 4, and

FIG.14 shows an example of a realization structure of some components of the circuit of FIG. 6.

FIG.1 shows an example of a structure of a semiconductor electronic device comprising a power stage and a control circuit in which are represented for the sake of simplicity only one component of the integrated control circuit, a low voltage npn transistor with emitter, base and collector terminals indicated by E_1, B_1 and C_1 respectively and a single power transistor also of the npn type and having emitter, base and collector terminals indicated by E_P, B_P and C_P respectively and in which E_P together with the "-" terminal of the supply battery is designed to be grounded (directly or through one or more passive components inside or outside the monolithic circuit).

In said FIG.1 represents a substrate of N+ doped semiconductor material, 2 an N doped layer and 3 an insulation region with P doping designed to insulate the individual components of the control circuit from each other and from the power transistor once its ISO terminal is also grounded so as to ensure that both the junctions of the parasite transistor associated with the insulation region are always reverse polarized.

In FIG.2 is diagramed the equivalent electric circuit of the structure of FIG. 1. It shows the npn vertical parasite transistor (Qvi) which, normally polarized with both the junctions reversed, ensures insulation between the vertical power transistor (Qpv) and the signal transistor (Qs1) of the pilot circuit provided inside the layer 3.

FIG.3 illustrates the basic diagram of the dynamic insulation circuit in accordance with the known art (French patent application no. 89/16144). Therein P represents a pilot circuit which detects the voltage level of the collector CP of the power transistor and holds the switch S1 (consisting of a vertical MOS transistor or a bipolar transistor) closed and the switch S2 (consisting of a lateral MOS transistor) open as long as said level is greater than the ground potential. As soon as said level falls transiently below said potential, P commands opening of S1 and simultaneously closing of the switch S2.

FIG.4a illustrates the basic diagram of the dynamic insulation circuit of the present invention. In accordance with said diagram the switch piloting circuit CPI detects, in addition to the voltage level of the collector C_P of the power transistor, the level of the collector C_1 of the control circuit. As long as the voltage of C_P and C_1 is greater than the voltage of the ground node, CPI holds the switch S1 closed and the switches S2 and S3 open. As soon as the potential of C_P or C_1 falls transiently below ground potential, CPI commands opening of S1 and closing of S2 or S3 respectively, i.e. it commands closing of the switch connected to the terminal from which arrives the most negative disturbance.

If in the integrated circuit there exist other terminals subject to transient subground situations, the solution described above still applies by adding to S2 and S3 a number of switches equal to the number of the added terminals.

The circuit of FIG.4a, whose reference potential is ground, calls for separate supply Vs of the circuit CPI designed to permit supply of CPI even during subground transients. This separate supply, without interruptions, can be for example achieved simply by keeping uniformly charged a capacitance designed to supply power to CPI during the transients.

The circuit of FIG.4b in comparison with that of FIG. 4a calls for use as reference potential that of the ISO terminal instead of ground.

FIG.5 shows the diagram of an example of embodiment of the circuit CPI of FIG. 4a in which A1 and A2 represent two voltage comparators and N a NOR logic circuit. The voltage generator VB compensates for the voltage drop on the diodes DA1, DA2.

FIG.6 shows the basic diagram of the dynamic insulation in accordance with the present invention applied to a solid state 2-way switch (QA/QB) integrated in a single semiconductor material chip. In this diagram there are omitted for the sake of simplicity (in comparison with FIG. 5) the switches S3A and S3B for connection of the nodes ISO A and ISO B with the collector and drain terminals of the respective control circuits. The power switches QA and QB are piloted by appropriate circuits inserted also in the pilot circuits A and B respectively and designed to perform the above function.

In this case the two insulation regions of the control circuits of the power transistors QA and QB are not connected together because the elementary components contained in them must be free to follow the potential imposed on SA and SB by two external sources.

To withstand the voltages applied (on the order of several hundred volts) QA and QB must be vertical transistors and therefore their drain (or collector if QA and QB are provided by bipolar transistors and not MOS transistors as indicated in FIG. 6) coincide with the substrate of the semiconductor chip in which they are provided.

In a configuration of this type if a generator of alternating electromotive force is applied between the two terminals SA and SB leading to the surface of the chip, the substrate will be alternately subjected to reversal of polarity in relation to the local ground nodes.

Dynamic insulation in accordance with the invention will then provide that, on command of the pilot circuit A, the insulation ISO A of the control circuitry of the switch QA is alternately connected to the more negative local potential S_A or to the potential D if it is more negative than S_A. Similarly the insulation ISO B will always be taken upon command of the pilot circuit B to the lower of the potentials S_B and D regardless of what happens for ISO A (in the figures GNDA and GNDB represent ground nodes, VsA and VsB separate power supplies, and VinA and VinB optional control inputs to synchronize piloting of QA and QB by means of an external logic circuit not shown in the figures).

In implementing the dynamic insulation principle in accordance with the present invention it is advantageous to provide at least the switch S1 with a metal gate NMOS transistor and with the channel region achieved by means of selective etching of a thick oxide layer grown on the surface of the slice followed by a subsequent growth of the gate oxide. Further advantages are achieved by providing both the switches S1 and S2 with metal gate NMOS transistors of the 'double diffused' type, i.e in which both the source region and the channel region are the diffused type (with the channel region having a nonuniform dopant concentration profile along the surface).

This manner of implementation of the switches S1 and S2 is advantageous based on the following considerations:

- the NMOS transistors switch faster than the parasite bipolar transistor of the insulation structure and consequently a conduction of the latter transistor is not possible during switching,
- the channel length of a double diffused NMOS transistor is determined by the difference in the lateral diffusions of the source and body regions contrary to a transistor with uniform concentration channel region, for which the channel length is defined by a photolithographic process,
- the double diffused NMOS transistor is capable of withstanding high voltages.

In FIG.7 is illustrated an example of a structure implementing the switches S1 and S2 of FIG. 4a and 4b with metal gate NMOS transistors of the 'double diffused' type and with channel region achieved beneath a thin oxide layer. In said figure So1, G1 and D1 represent the source, gate and drain terminals of the transistor implementing the switch S1 while So2, G2 and D2 represent the homologous terminals of the transistor implementing the switch S2.

FIGS.8 to 11 illustrate the processing sequence which consists of the following phases:

1) growth of an n- epitaxial layer 2 on a monocrystalline substrate 1 of the same type of conductivity and low resistivity,

2) formation of the horizontal region 3 for insulation of the integrated control circuit (p-buried layer) of type p and of the collector region 4 with low resistivity of an npn transistor of the integrated control circuit (n-buried layer) of type n (this region acts as the low resistivity drain region of the NMOS transistor implementing S1),

3) growth of a second epitaxial layer 5 of type n-,

4) definition of the insulation regions 6 of type p+ and sink 7 of type n+ necessary for connecting to the surface of the device the horizontal insulation region and the low resistivity collector region respectively of an npn transistor of the integrated control circuit,

5) formation of the deep body region 8 of the NMOS transistor (which coincides with the base region of the npn transistor of the integrated control circuit),

6) formation of the body region 9 of the NMOS transistor (FIG. 9),

7) formation of the source region 10 of the NMOS transistor, coinciding with the emitter region of the npn transistor of the integrated control circuit (FIG. 10),

8) definition of the channel regions by selective etching of the thick oxide 11 and subsequently growth of the gate oxide 12 (FIG. 11),

9) opening of the contacts, provision of the metalization paths (with gate electrode function for the NMOS transistors in addition to interconnection of the device components) and finally metalization of the back thereof (FIG. 7).

It is observed that, since only the switch S2 is subject to high voltages, the switch S1 can be provided (as exemplified in FIG.12) even by an

NMOS transistor with uniform concentration channel region.

The process described above for the structure of FIG. 7 can be used in this case also, if there is provided a different layout for the deep body, body and source photomasking for the NMOS transistor implementing S1 (source and drain of the NMOS transistor are achieved using the same emitter diffusion of the npn transistor of the integrated control circuit and the buried type n layer is short-circuited with the channel region).

This variant of the structure in accordance with the present invention allows separate optimization of the channel regions of the two NMOS-FETs (it is possible for example to provide two different threshold voltages).

One possible shortcoming of the NMOS structures could be the Ron of the high voltage transistor (switch S2). Indeed, it is known that unipolar devices do not enjoy the phenomenon of conductivity modulation and therefore the voltage drop between source and drain of this transistor can be high.

Under these conditions it is possible that, when the voltage Vout of the terminal CP is negative (and hence S2 is closed) between it and the insulation is established a potential differential greater than necessary for turning on the parasite bipolar transistor, which is equal to approximately 0.5V at 27°C. Turning on the parasite transistor is prevented by the present invention and in FIG.13 is shown implementation of the switch S2 (of the circuit of FIG. 5) with a bipolar transistor and implementation of S1 with a metal gate NMOS transistor with uniform concentration channel region.

The voltage applied to the insulation region differs from Vout (when Vout is negative) by one Vcesat, i.e. a quantity less than that necessary to turn on the parasite bipolar transistor associated with the insulation region.

In FIG.14 is diagramed a possible structure providing, in accordance with the above criteria, some components of the circuit of FIG. 6 and in particular the switch pair $S1_A$ and $S2_A$ and the switch QA as well as the insulation region ISO_A (the structure of the corresponding components $S1_B$, $S2_B$, Q_B and the region ISOB is the same).

In the figures the meaning of the various symbols is as follows:
CH: channel stop region terminal
A: anode of DA
while the other abbreviations G(), S(), D() represent the gate, source and drain respectively of the transistor implementing the switch indicated in parentheses.

The drain terminal $D(S1_A)$ is grounded and the MOS transistor which provides the switch $S1_A$, which in a state of conduction has the source region more positive that the drain region, can in this manner support the negative transistors in a state of interdiction without the drain-body diode of said transistor going into conduction.

It is clear that to the examples of embodiments described above by way of nonlimiting illustration can be made numerous modifications, adaptations, variants and replacements of elements by other functionally equivalent ones without thereby going beyond the protective scope of the claims set forth below.

One such variant could for example affect the circuits of FIGS. 4a and 4b since the switch S3 and the circuit CP/CPI can be connected with another region of said transistor instead of with the collector C_1 of the control circuit transistor.

Claims

1. Semiconductor electronic device with dynamic insulation circuit comprising at least one power transistor and at least one control circuit integrated monolithically in the same chip wherein there is present:
   - an insulation region designed to insulate the individual components of said control circuit from each other and from the power transistor,
   - a first switch designed to connect the insulation region with a ground node,
   - a second switch designed to connect the insulation region with the collector or drain of the power transistor,
   - a pilot circuit connected with the collector or drain of the power transistor, with the ground node and with the above sain first and second switch which, depending on whether the above collector or drain has potential greater or smaller respectively than that of ground, commands closing of the first or second switch respectively,

   characterized in that:
   - there is present a third switch (S3) designed to connect the insulation region with a region of a control circuit transistor,
   - the pilot circuit is connected with said third switch (S3) and with said region of said control circuit transistor and commands closing of the third switch (S3) and opening of the first (S1) when said region of said control circuit transistor has potential less than that of ground.

2. Semiconductor electronic device with dynamic insulation circuit comprising at least one power transistor and at least one control circuit in-

tegrated monolithically in one chip in which is present:

- an insulation region designed to insulate the individual components of said control circuit from each other and from the power transistor,
- a first switch designed to connect a node of the insulation region with a ground node,
- a second switch designed to connect said insulation node with the collector or drain of the power transistor,
- a pilot circuit connected with the collector or drain of the power transistor, with the ground node and said first and second switches, which, depending on whether said collector or drain has potential greater or smaller respectively than that of said insulation region, commands closing of the first or second switch respectively,

characterized in that:

- there is present a third switch (S3) designed to connect the insulation region with a region of a control circuit transistor,
- the pilot circuit is connected with said third switch (S3) and with said region of said control circuit transistor and commands closing of the third switch (S3) and opening of the first (S1) when said region of said control circuit transistor has potential less than that of the insulation region.

3. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 1 or 2 characterized in that said first switch (S1) is provided by a metal gate NMOS transistor with the channel region achieved beneath a thin layer (12) of oxide grown on the surface of the slice.

4. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 3 characterized in that said NMOS transistor providing the first switch (S1) is the double diffused type.

5. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 4 characterized in that said second switch (S2) is also provided by a metal gate NMOS transistor of the double diffused type with the channel region achieved under a thin layer (12) of oxide grown on the surface of the slice.

6. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 4 characterized in that said first switch (S1) is provided by a metal gate NMOS transistor with uniform concentration channel region achieved under a thin layer (12) of oxide grown on the surface of the slice.

7. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 3 characterized in that said NMOS transistor providing the first switch (S1) is the uniform concentration channel type and the second switch (S2) is provided by a bipolar transistor.

8. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 3 characterized in that in said pilot circuit (CPI) are present in combination:

- a NOR logic circuit (N) whose output (D1) pilots said first switch (S1),
- a first and a second voltage comparator (A1,A2) whose "-" inputs are connected with said region of said control circuit transistor and of said power transistor respectively whose "+" inputs are connected with said ground or insulation node (ISO) and whose outputs pilot a third switch (S3) and a first input of said NOR circuit (N) and a second switch (S2) and a second input of said NOR circuit (N) respectively.

9. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 3, present in the framework of a structure comprising two power switches (QA,QB) implemented by vertical transistors with source or emitter terminal (S_A,S_B) in common with ground (GNDA,GNDB) of the respective pilot circuit, providing a 2-way switch and each equipped with a respective control circuit (A,B) with insulation regions not connected together, used to connect the terminal (ISO_A,ISO_B) of the insulation region of each control circuit to said source or emitter terminal (S_A,S_B) or to the collector or drain terminal (DA,DB) of the respective power switch (QA,QB) depending on whether the source or emitter terminal (S_A,S_B) has potential less or greater than respectively said collector or drain terminal (DA,DB).

10. Semiconductor electronic device with dynamic insulation circuit as set forth in claim 9 characterized by the presence of two additional switches (S3A,S3B) capable of connecting the terminal of the insulation regions of each control circuit with the collector or drain terminal of

a transistor of the respective control circuit if the latter is more negative than the common collector/drain (D) or the source or emitter terminals (S_A,S_B).

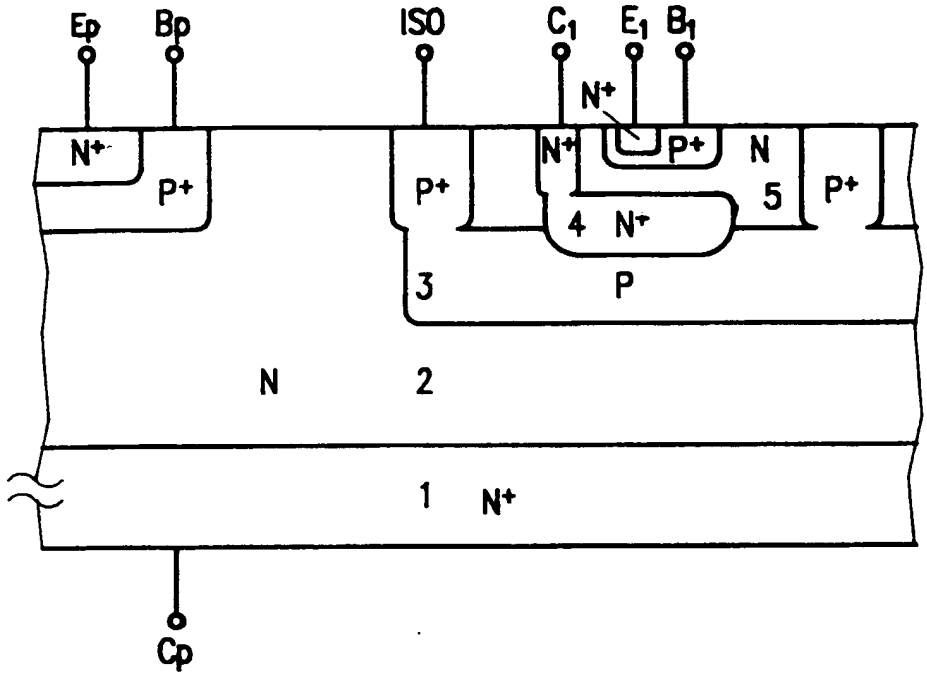


Fig. 1

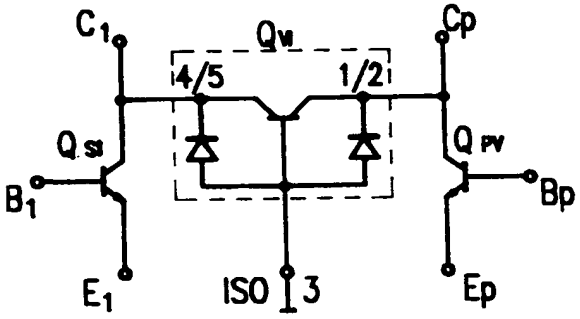


Fig. 2

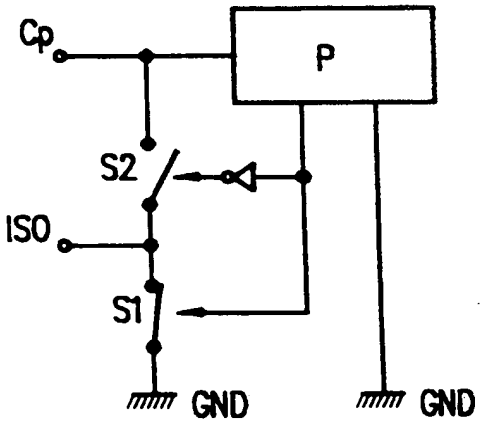


Fig. 3

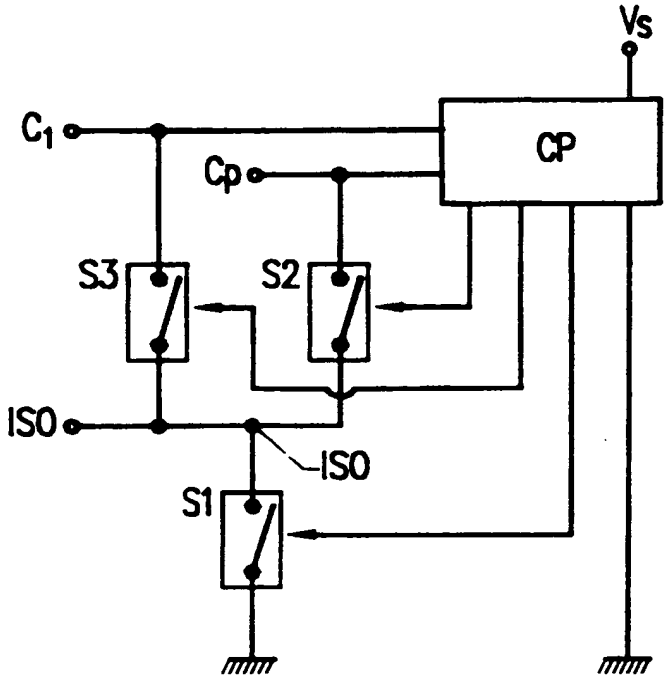


Fig. 4a

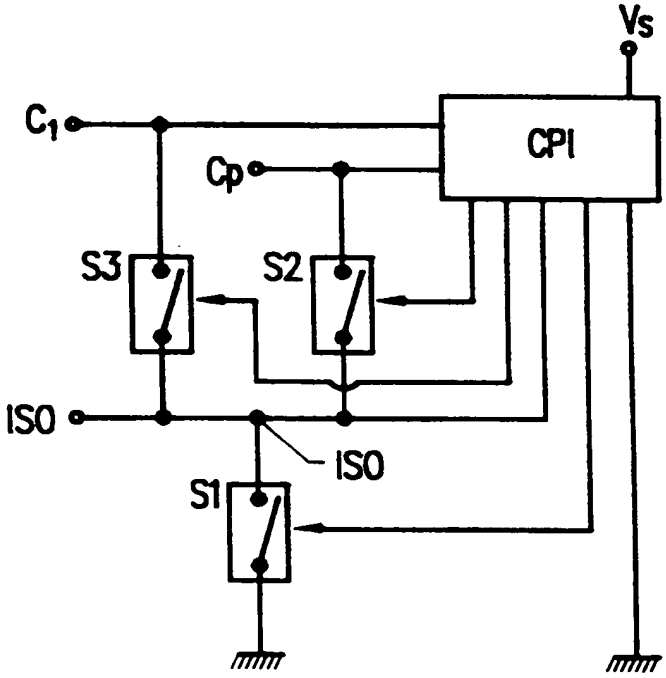


Fig. 4b

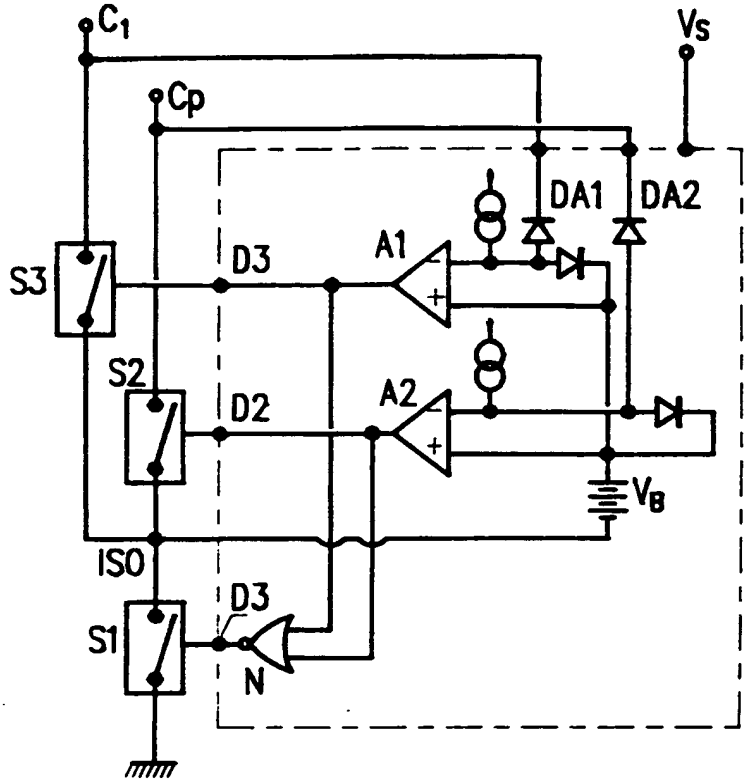
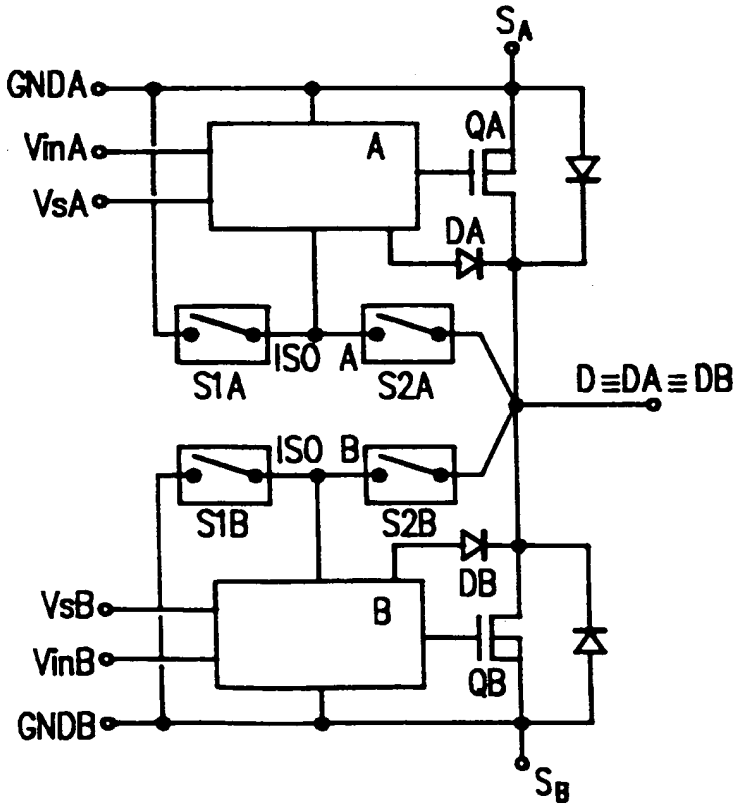

C1
Vs
Cp
DA1
DA2
S3
D3
A1
S2
D2
A2
VB
ISO
D3
S1
N

Fig. 5


SA
GNDA
VinA
VsA
A
QA
DA
S1A
ISO
A
S2A
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ISO B
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VsB
VinB
GNDB
B
QB
SB

Fig. 6

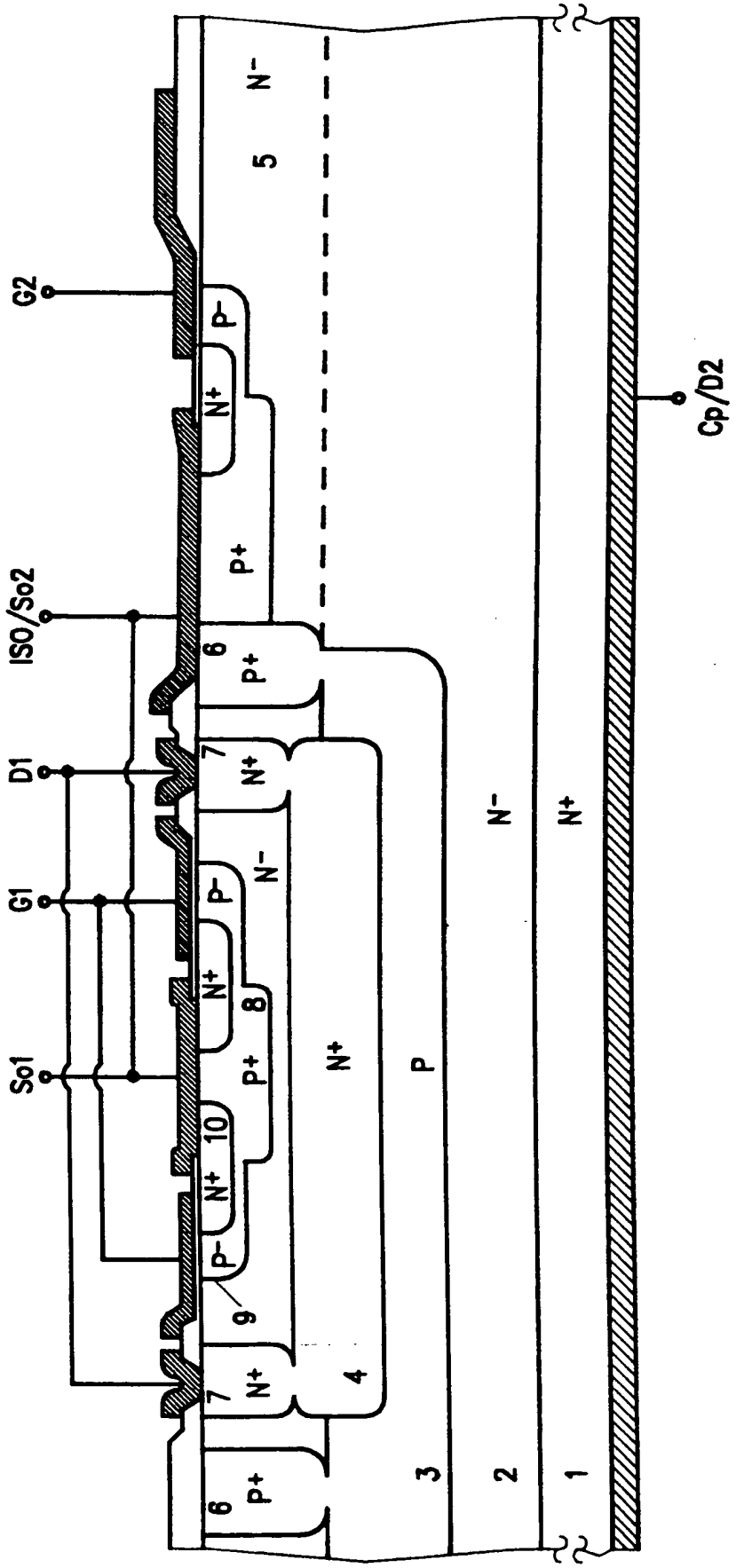

Fig. 7

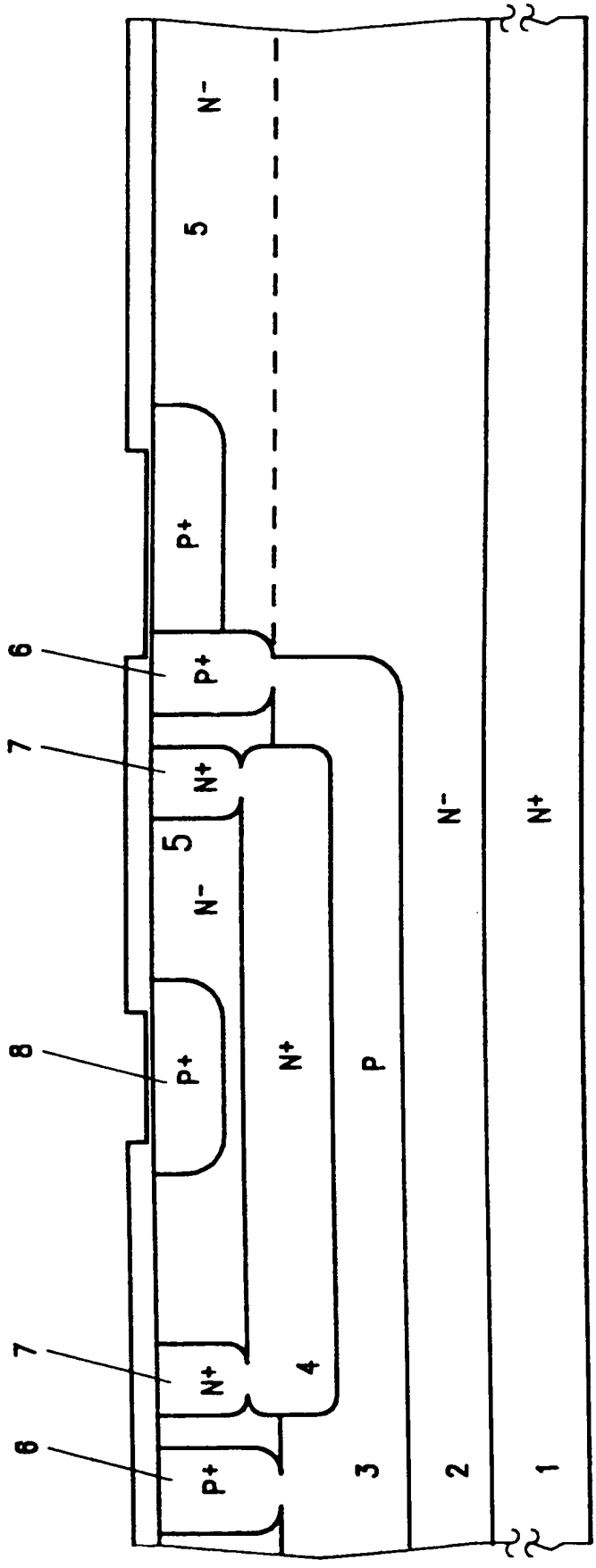

Fig. 8

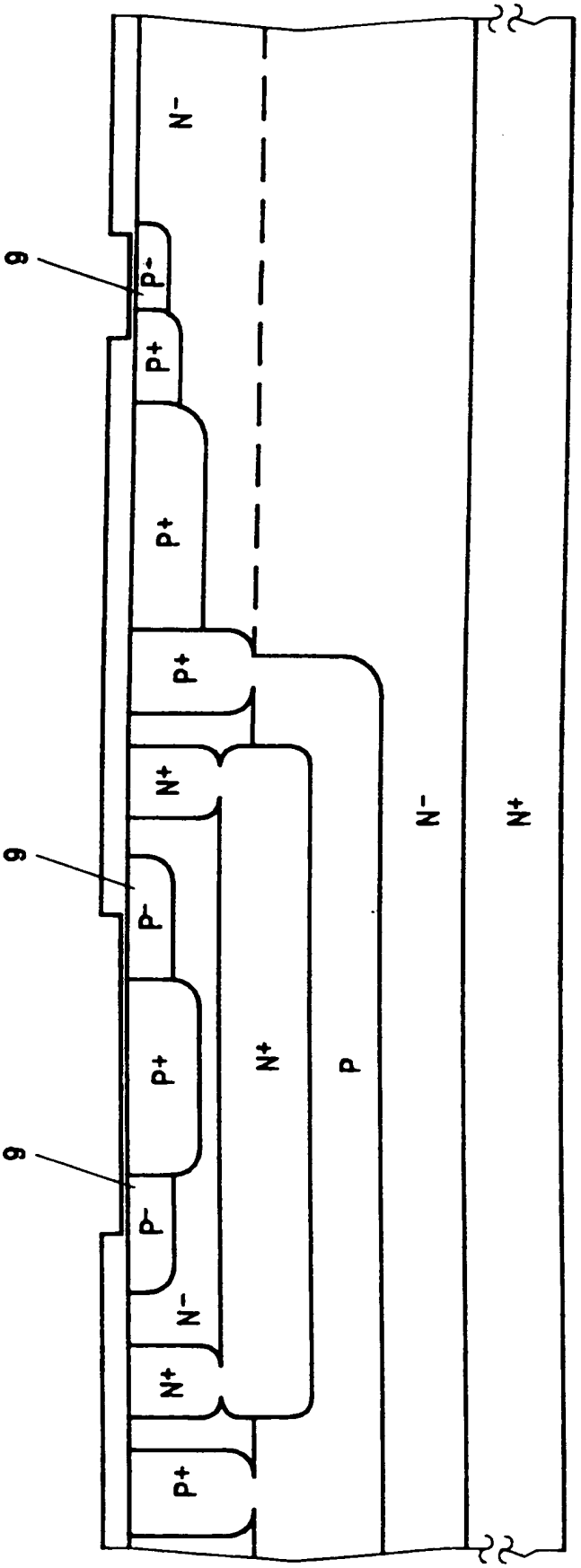

Fig. 9

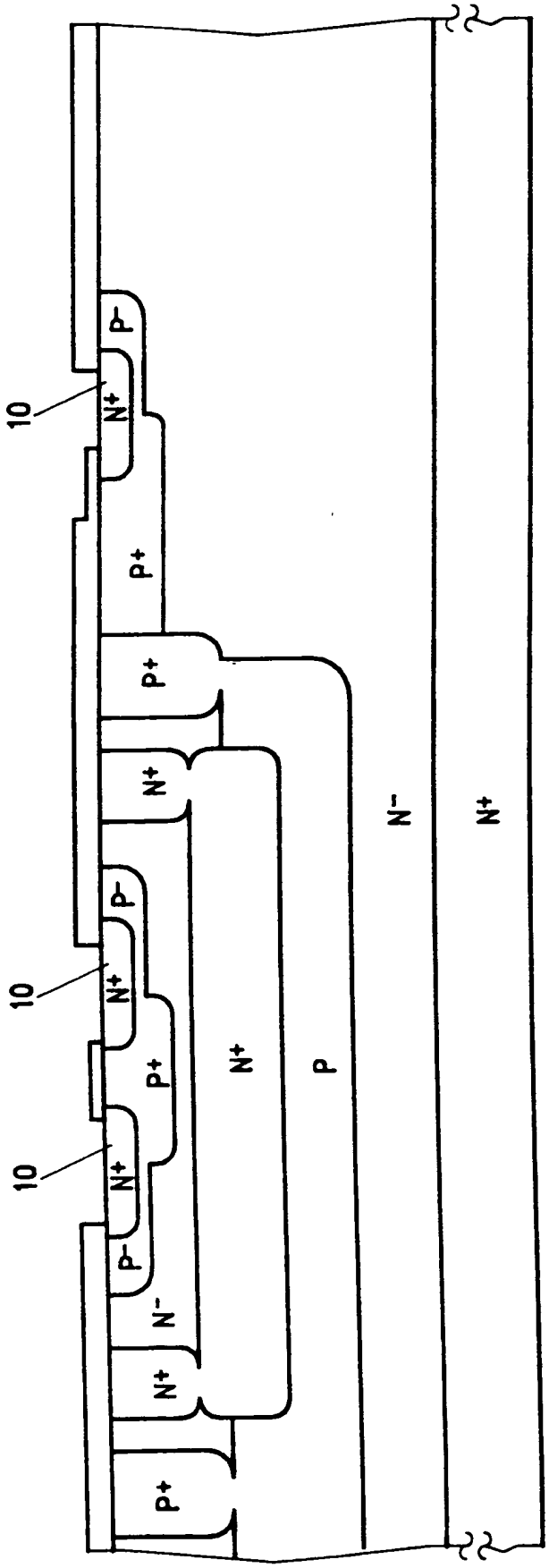

Fig. 10

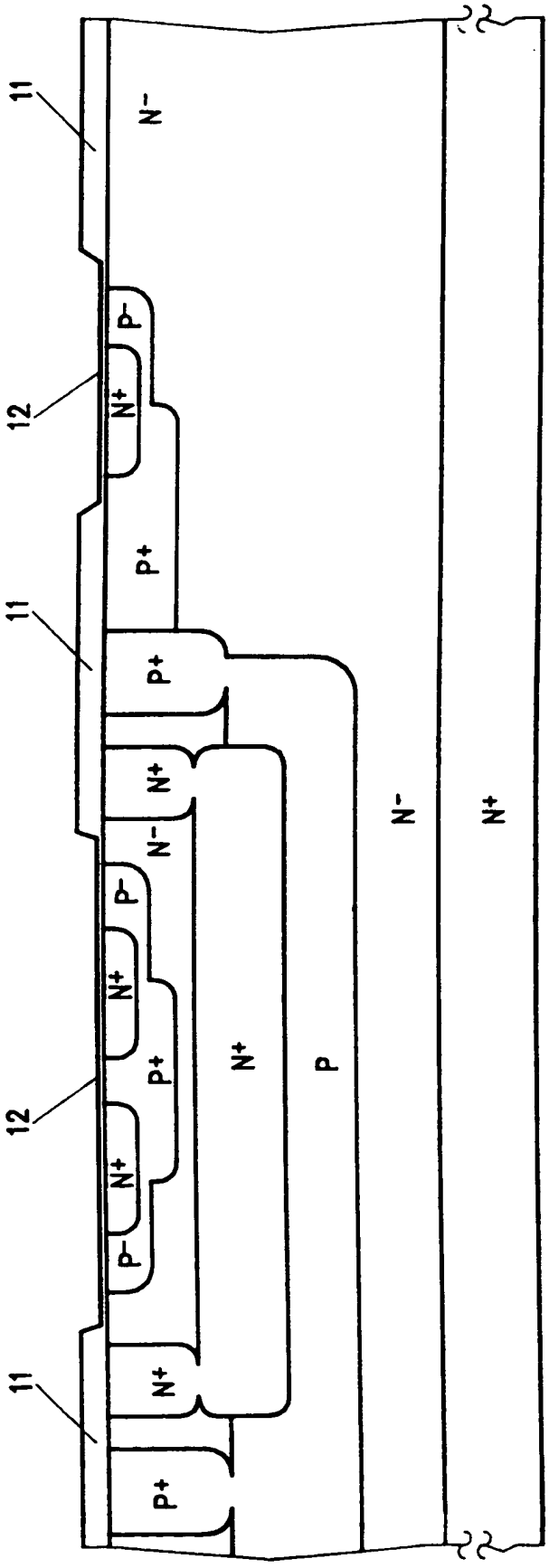

Fig. 11

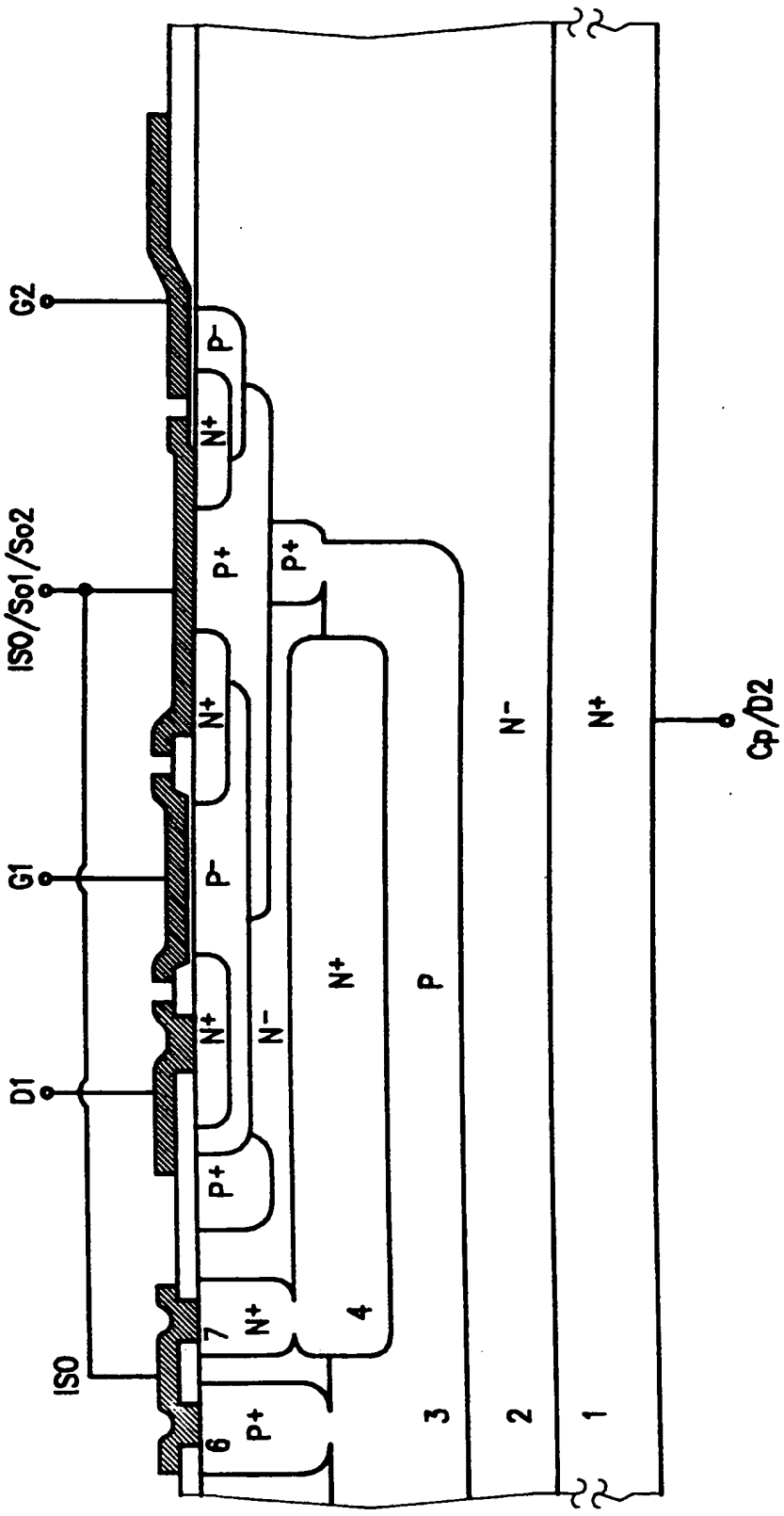

Fig. 12

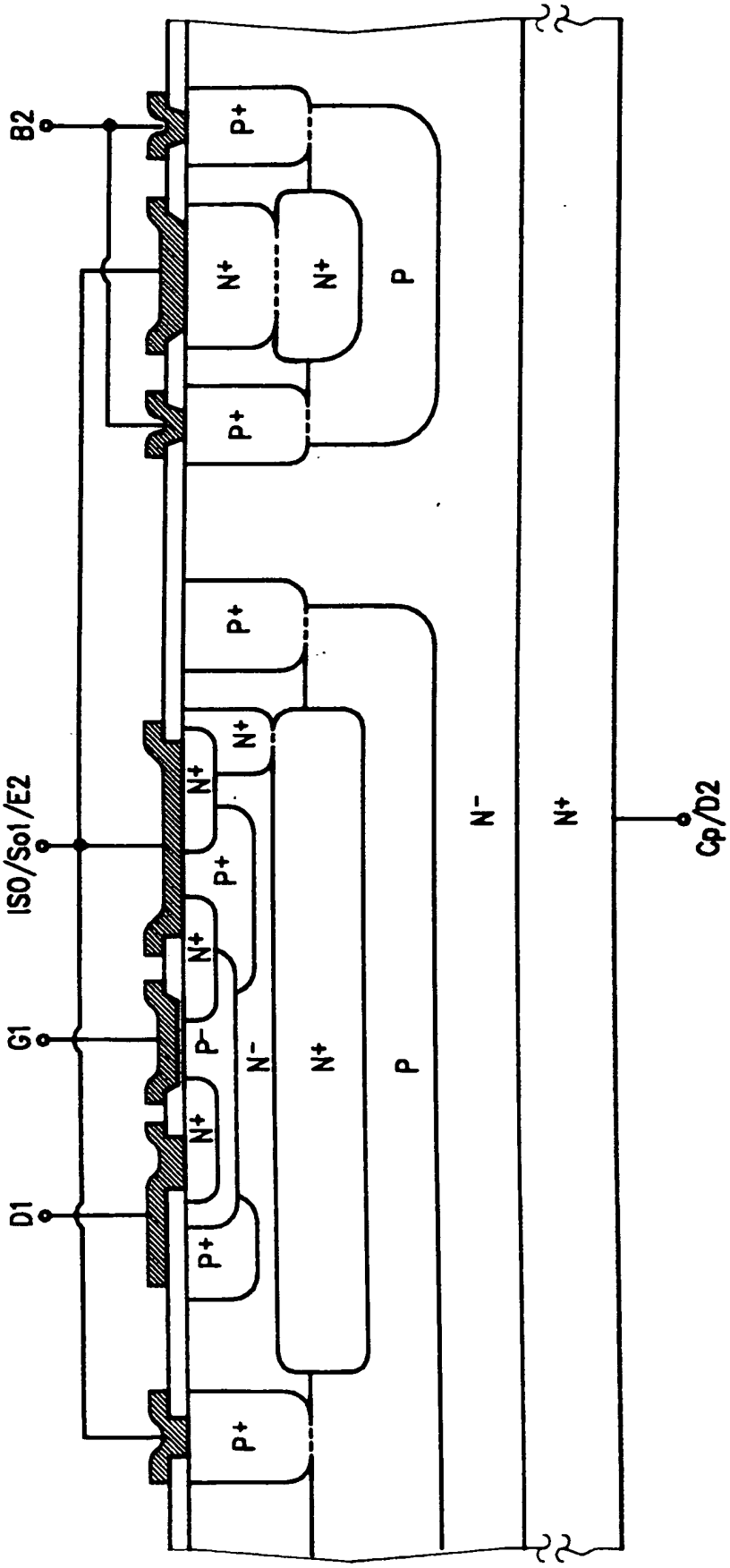

Fig. 13

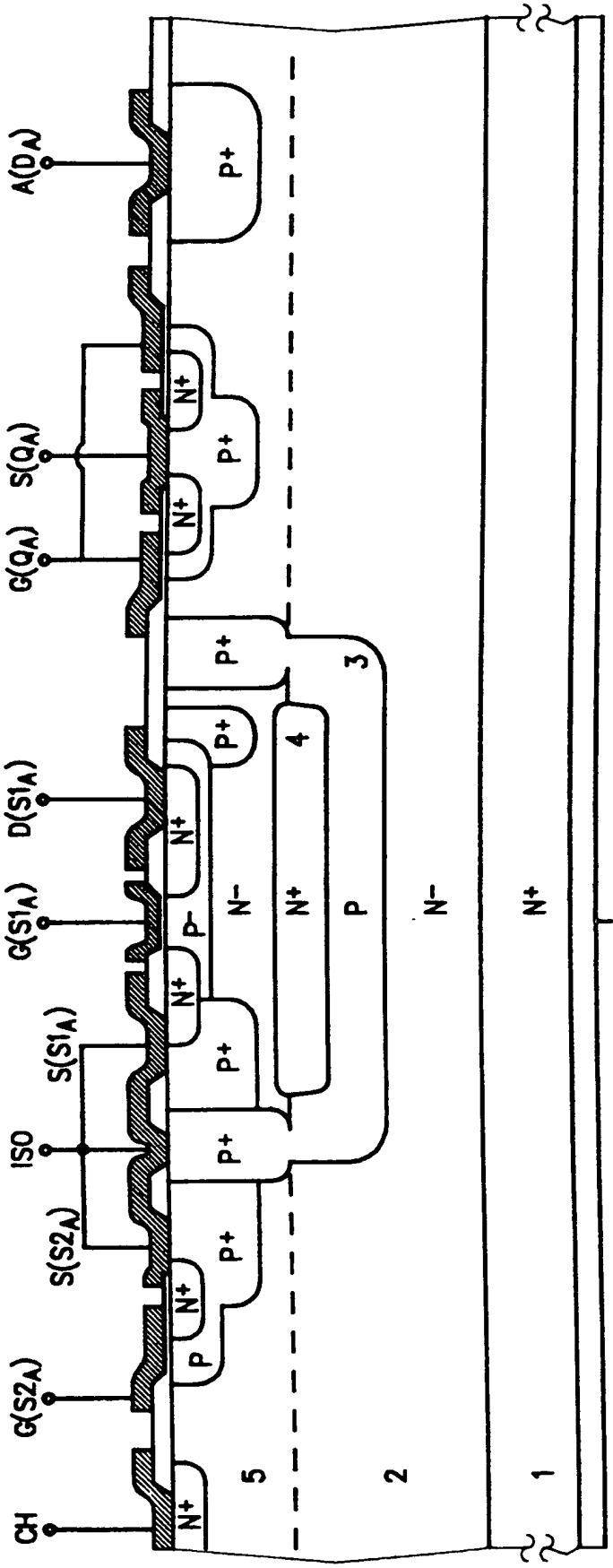
A(DA)
S(QA)
G(QA)
D(S1A)
G(S1A)
S(S1A)
ISO
S(S2A)
G(S2A)
CH
P+
N+
P
P-
N-
5
2
1
3
4
D (S2A) ≡ D (QA)

Fig. 14

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 20 3677

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-5 051 612 (TEXAS INSTRUMENTS INC.) 24 September 1991 * column 4, line 5 - column 6, line 12; claims 5,12-19; figures 8-14 *	1-2	H01L27/02
D,A	EP-A-0 432 058 (SGS-THOMSON-MICROELECTRONICS S.P.A.) 12 June 1991 * claims 1,7-8; figure 4 *	1-2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 MARCH 1993	FRANSEN L.J.L.

CATEGORY OF CITED DOCUMENTS

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